Amendments In The Specification

☞ Page 10, please **replace** the first full paragraph (after the title and heading) with:

-- The subject matter of the present Application includes a transition detection circuit usable in a logic analyzer adapted to perform eye diagram measurements, or in a stand-alone circuit for that purpose. And although we disclose herein the general nature of such a detector in sufficient detail to allow a complete understanding of the invention, the actual circuit has complexity beyond what is needed here and is capable of performing additional functions. That actual circuit is the subject matter of a US Patent ~~Application~~ 6,463,392 entitled System and Method for Adjusting a Sampling Time in a Logic Analyzer, ~~of S/N 09/375,307,~~ filed on 16 August 1999 by Richard A. Nygaard et. al, issued 8 October 2002 and assigned to Agilent Technologies, Inc. Because the subject matter of that Application is of interest to that of the present invention, and for the sake of brevity herein, "System and Method for Adjusting a Sampling Time in a Logic Analyzer" is hereby expressly incorporated herein by reference. --;

☞ Pages 3 & 4, please **replace** the first full paragraph beginning on page 3 (and ending on page 4) with:

-- A logic analyzer can be equipped to perform eye diagram measurements by equipping each SUT clock signal input and each SUT data signal input channel with individually variable delays in their respective signal paths. If the range of signal delay is, say, n-many SUT clock cycles, then the SUT clock signal delay might be set at about n/2. For each data channel that is to undergo eye diagram measurement, there is specified some combination of a point in time relative to an instance of the delayed clock signal (data signal delay) and a voltage threshold. The specified combination (data signal delay, threshold) is essentially a location on an eye diagram, although the trace may or may not ever go through that location. There is also specified how many times this specified combination will be watched before another such combination is invoked. As the SUT runs, a particular specified combination will occur always, sometimes or never. A counter counts the number of SUT clock cycles used as instances of the reference for the eye diagram, and another counter counts the number of times the specified combination of conditions was met (hereinafter called "hits"). After watching a specified combination for the requisite length of time or number of events, the number of SUT clock cycles involved and the associated number

of hits are stored in memory using a data structure indexed by the components of the specified combination (data signal delay, threshold and which channel). Next, a new combination of data signal delay and threshold is specified and a measurement taken and recorded in the data structure. The process is repeated until all possible combinations within a stated range of data signal delay and threshold voltage (using specified resolution/step sizes for delay and voltage) have been investigated. The range of data signal delay might be ~~a~~as large as from zero to n-many SUT clock cycles (which would be n/2 before and after the delayed reference), or it could be some lesser amount. As this process proceeds under the control of firmware within the logic analyzer, other firmware can be examining the data structure and generating a partial eye diagram visible on a display, and that will be complete soon after the measurement itself is finished. This technique can also be used to implement a stand alone eye diagram analyzer. --;

☞ Page 6, please **replace** the first full paragraph with:

-- Refer now to Figure 2, which is a simplified block diagram 9 of ~~an eye diagram analyzer, which~~ may be either a stand-alone unit or incorporated into a logic analyzer (additional details for which are not shown). At the core of the block diagram ~~1~~9 is some EYE DIAGRAM ACQUISITION HARDWARE 10, which receives an SUT clock signal 18 and one to n-many SUT data signals (19) for which eye diagram measurements are desired. In a logic analyzer setting there may be upwards of one hundred and twenty SUT data signals. --;

☞ Page 12, please **replace** the first full paragraph with:

To resume the discussion of how to make a run, each channel further delays its copy of the real delayed clock signal 46 to produce a doubly delayed clock signal 45. This is accomplished by a dt delay circuit 44 of, say, four tapped delays of 70 ps, 120 ps, 170 ps and 220 ps . The doubly delayed clock signal 45 clocks a latch 48 whose D input is also the (same) delayed data signal applied to latch 47. The idea is that if the two latches 47 and 48 have different values (detected by XOR gate 49) after both have been clocked, then the SUT DATA INPUT SIGNAL 34 must have transitioned through V_T sometime during the interval between when latch 47 was clocked and latch 48 was clocked. Accordingly, it will be noted that in Figure 4 this collection of circuitry is termed a TRANSITION DETECTOR (42). We have

called that time interval dt in connection with Figures 1 and 3. The value of dt is the delay provided by the dt delay circuit 44. --; and

☞ Pages 12 & 13, please **replace** the final paragraph beginning on page 12 and continuing onto page 13 with:

At this time the value 52 accumulated in the # OF HITS COUNTER 51 is stored by the EDA system in the indexed location of the data structure, along with any other information deemed useful, such as the value 54 of the pre-load for counter 53. It will be noted that the block diagram 24 suggests that this happens in an instance by instance manner. It will also be appreciated, however, that while the block diagram ~~give~~gives the proper functionality to be obtained, it is often desirable for performance reasons to employ additional techniques such as pipelines, parallelism and MUX'ing of cached results to 'get things to run faster than they really do'.. --.